REMARKS

The above amendments and these remarks are in reply to the Final Office Action mailed on September 19, 2002.

I. **Election/Restriction:**

The present Office Action states:

> "The newly submitted claims 18-22 are directed to an invention that is independent or distinct from the invention originally claimed invention for the following reasons:
>
> - Species I: a semiconductor device, wherein an erase gate is formed over sidewalls of one floating gate, as shown in Figure 1.
> - Species I: a memory array wherein an erase gate is formed over portions of both first and second floating gates as shown in Figure 2."

(Final Office Action at page 2.)

Responsive to the Examiner's Requirement under 35 U.S.C. § 121 that a single disclosed species be elected for prosecution on the merits, Applicants provisionally elect with traverse to prosecute the invention of Species I, which includes Figure 1, upon which claims 1, 2, 8-10 and 16 read.

A. **Traversal of Requirement for Election of Species:**

Applicants respectfully request reconsideration of the instant requirement for election of species. Applicants hereby preserve the instant request for reconsideration for subsequent petition and appeal.

Applicants believe that each of independent claims 1, 8 and 16 of the present application reads on, and is generic to, the subject matter depicted in each of Figures 2 through 6 of the present application. The Examiner has characterized the claims identified as being part of Species I (claims 1, 8 and 16 of the present application) as being limited to "a semiconductor device, wherein an erase gate is formed over sidewalls of one floating gate." (Final Office Action at page 2.) Applicants respectfully submit that claims 1, 8 and 16 of the present application are not limited to having an erase gate formed over sidewalls of only ***"one"*** floating gate. Rather, each of claims 1, 8 and 16 of the present application should be understood to refer to "an erase gate formed over ... [*at least one*] ... floating gate." As properly construed, each of

claims 1, 8 and 16 of the present application reads on, and is generic to, the subject matter depicted in each of Figures 2 through 6 of the present application.

Therefore, Applicants submit that the present Restriction Requirement is not justified under 35 U.S.C. § 121. Withdrawal of the instant requirement for restriction is appropriate. Accordingly, Applicants respectfully request that the requirement be withdrawn and that the entire application be examined on the merits.

II. **Rejections of Claims Currently Being Considered:**

Claims 1, 2, 8-10 and 16-22 are now pending. As explained, claims 18-22 are currently withdrawn from consideration by the Examiner as being drawn to a non-elected species. Claims 1, 2, 8-10 and 16-17 have been rejected under 35 U.S.C. §112 as being indefinite. Claims 8 and 9 have been rejected under 35 U.S.C. §102(b) as being anticipated by Eitan et al. (U.S. Patent Number 4,998,220). Claims 1, 2, 8-10 and 16-17 have been rejected under 35 U.S.C. §103(a) as being obvious over Eitan et al. in view of Chang et al. (U.S. Patent Number 6,126,060).

Applicants respectfully traverse each of the rejections as explained below. Claims 1, 9 and 16 have been amended in order to overcome the rejections as explained below. Support for amended claims 1, 9 and 16 is found in the specification of the originally filed application. No new subject matter has been added. Applicants thank the Examiner for careful review of the claims.

A. **Rejections under 35 U.S.C. § 112**

Claims 1, 2, 8-10 and 16-17 have been rejected under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as their invention. In particular, the Examiner pointed out that use of the term "generally" to describe the relative positions of various gates and regions - was indefinite. Applicants disagree with the Examiner on this point because "generally disposed over" is well understood by those of ordinary skill in the art to mean "having at least a substantial portion thereof disposed over." However, as indicated above, Applicants have amended claims 1, 9 and 16 to replace the phrase "generally disposed over" with the phrase "having at least a substantial portion thereof disposed over," and to replace the phrase "generally [placed or disposed on a] side of" with the phrase "substantially [placed or disposed on a] side of."

The Examiner has suggested that "[i]t seems that Applicant, by using this term ["generally"], is acknowledging that the claimed device is well known in the art." (Final Office Action at page 2.) Applicants strongly disagree with this suggestion. The term "generally" does not convey anything whatsoever about the knowledge of those of ordinary skill in the art regarding either the claimed invention as a whole or any portion of the claimed invention. To the contrary, the previous uses of the term "generally" only described the relative positions of various gates and regions of the claimed devices. As already mentioned, Applicants have amended claims 1, 9 and 16 to more particularly point out and distinctly claim the relative positions of various gates and regions of the claimed devices. Applicants do not intend to limit the scope of the claim or the range of equivalents by virtue of any of the above-described amendments. Applicants thank the Examiner for careful review of the claims.

B. **Rejections under 35 U.S.C. § 102**

Claims 1 and 16 have been rejected under 35 U.S.C. §102(b) as being anticipated by Eitan et al. As pointed out by the Examiner, Eitan et al. teaches an electrically erasable programmable read only memory (EEPROM) having an erase gate extending over a portion of a floating gate.

However, the Examiner acknowledges that Eitan et al. fails to teach "an erase gate formed over a second one of said side walls ... of said floating gate" as recited in each of the independent claims 1 and 16. (Final Office Action at page 7.) Applicants also assert that Eitan et al. does not disclose an apparatus as recited in independent claims 1, 8 and 16. In particular, Eitan et al. fails to teach that "... ***during an erase operation ... the source region ...*** [is] ***connected to ground.***" (*See* each of the independent claims 1, 8 and 16.) Instead, Eitan et al. teaches that during an erase operation, a voltage of 12 volts is applied to the source region. (Eitan et al. at col. 7, lines 44-58.) Therefore, Eitan et al. actually teaches away from connecting the source region to ground during an erase operation.

For a prior art reference to anticipate in terms of 35 U.S.C. §102, every element of the claimed invention must be identically shown in a single reference." In re Bond, 910 F.2d 831 15 USPQ2d 1556 (Fed. Cir. 1990.) Because Eitan et al. fails to teach "an erase gate formed over a second one of said side walls" and connecting the source region to ground during an erase

operation, it is clear that Eitan et al. does not anticipate the invention recited in each of the independent claims 1 and 16.

C. **Rejections under 35 U.S.C. § 103(a)**

Claims 1, 2, 8-10 and 16-17 have been rejected under 35 U.S.C. §103(a) as being obvious over Eitan et al. in view of Chang et al. Applicants assert that neither Eitan et al. nor Chang et al., either individually or collectively disclose an apparatus as recited in independent claims 1, 8 and 16. The Examiner acknowledges that Eitan et al. fails to teach "an erase gate formed over a second one of said side walls ... of said floating gate" as recited in each of the independent claims 1 and 16. (Final Office Action at page 7.) However, the Examiner finds the element of "an erase gate formed over a second one of said side walls ... of said floating gate" in the teaching of Chang et al. and asserts that "it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Eitan et al. to include an erase gate formed over a top and a sidewall of the floating gate." (Id.)

Applicants assert that neither Eitan et al. nor Chang et al., taken individually or collectively, discloses an apparatus wherein "... ***during an erase operation ... the source region*** ... [is] ***connected to ground***." (*See* each of the independent claims 1, 8 and 16.) Eitan et al. actually teaches away from connecting the source region to ground during an erase operation because it teaches that during an erase operation, a voltage of ***12 volts*** is to be applied to the source region. (Eitan et al. at col. 7, lines 44-58.) Similarly, Chang et al. teaches away from connecting the source to ground during an erase operation by teaching that the "source 105 is biased at ***an intermediate voltage*** (around Vcc)" during the erase operation. (Chang et al. at col. 6, lines 39-42.)

Applicants assert that claims 1, 8 and 16 as now recited, satisfy the requirements of 35 U.S.C. §103(a). MPEP 2143.03 states that: "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988). Independent claims 1, 8 and 16 are patentable under 35 U.S.C. §103(a) over Eitan et al. in view of Chang et al. Claims 2 and 17 depend from patentable claims 1 and 16 respectively, and as such incorporate all of the limitations of independent claims 1 and 16 rendering them patentable also. Likewise claims 9-10 depend from patentable claim 8 rendering them patentable also.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Applicant believes all the pending claims are now in condition for allowance. Applicant respectfully requests the amendments to the claims be entered and an early notice of allowance be provided.

Should a telephone conference be required to expedite the prosecution of this application, the Examiner is respectfully requested to contact the undersigned at the number set out below.

Respectfully submitted,

Dated: December 13 2002

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CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited on December 13, 2002, with the U.S. Postal Service as first class mail in an envelope addressed to: Box RCE, Commissioner for Patents, Washington, D.C. 20231.

Date: December 13, 2002

Yolette Yurralde-Owen

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region defined thereon;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate [generally] having at least a substantial portion thereof disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a first portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulation layer;

a drain region formed in a portion of said substrate proximate said control gate; and

a source region formed in a portion of said substrate proximate said erase gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

9. (Amended) A memory array disposed on a substrate as recited in claim 8 wherein said floating gate [is generally] has at least a substantial portion thereof disposed over said channel

region and is separated therefrom by said first insulating layer, said control gate is [generally] substantially placed on one side of said floating gate and separated therefrom by said second insulation layer, said erase gate is [generally] substantially placed on a second side of said floating gate and is separated therefrom by said second insulation layer, said drain region is [generally] substantially disposed on said one side of said floating gate, and said source region is [generally] substantially disposed on said second side of said floating gate.

16. (Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate [generally] having at least a substantial portion thereof disposed over disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a first portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first one of said side walls;

an erase gate formed over a second one of said side walls and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulation layer;

a source region formed in a portion of said substrate proximate said erase gate; and

a drain region formed in a portion of said substrate proximate said control gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored

electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.